Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims:

1-9. (cancelled)

10. (currently amended) A semiconductor device comprising a transistor channel, wherein:

the channel comprises an inner portion and an outer portion;

the outer portion surrounds the inner portion; ~~and~~

the inner portion and the outer portion have different lattice properties~~.~~; and

a gate formed over the channel, wherein the gate surrounds at least a section of the channel on at least three sides.

11. (original) The apparatus of claim 10, wherein the inner portion comprises silicon-germanium and the outer portion comprises silicon.

12. (original) The apparatus of claim 10, wherein the outer portion surrounds the inner portion on at least three sides.

13. (cancelled).

14. (currently amended) The apparatus of claim ~~13~~ 10, wherein the gate is substantially perpendicular to the channel.

15. (cancelled)

16. (currently amended) The apparatus of claim ~~13~~ 10, wherein a gate oxide is formed between the channel and the gate.

17. (currently amended) The apparatus of claim ~~13~~ 10, wherein a metal suicide layer is formed on a top surface of the gate.

18. (original) The apparatus of claim 10, wherein the thickness of the inner portion is between 10 nm and 90 nm.

19. (original) The apparatus of claim 10, wherein the thickness of the outer portion is between 10 nm and 100 nm.

20. (currently amended) The apparatus of claim 10, wherein the outer portion includes a layer ~~is~~ formed between the inner portion and the semiconductor substrate.

21. (original) The apparatus of claim 20, wherein the layer comprises silicon.

22. (original) The apparatus of claim 21, wherein the layer is strained silicon.

23. (original) The apparatus of claim 20, wherein the layer comprises approximately the same lattice property as the outer portion.

24. (original) The apparatus of claim 20, wherein the thickness of the layer is between 10 nm and 30 nm.

25. (original) The apparatus of claim 20, wherein:

the semiconductor substrate comprises a source region and a drain region; and

the channel is coupled to the source region and the drain region.

26. (new) A semiconductor device, comprising:

a substrate;

a channel having an inner portion and an outer portion formed on the substrate, wherein the inner portion and the outer portion have different lattice properties; and

a gate formed over the channel, and wherein the gate surrounds at least a section of the channel on at least three sides.

27. (new) The apparatus of claim 26, wherein a gate oxide is formed between the channel and the gate.

28. (new) The apparatus of claim 26, wherein the gate is substantially perpendicular to the channel.

29. (new) A semiconductor device, comprising:

a substrate;

a channel having an inner portion and an outer portion formed on the substrate, wherein the inner portion and the outer portion have different lattice properties;

a gate formed over the channel, and wherein the gate surrounds at least a section of the channel on at least three sides; and

a source region and a drain region coupled to the channel.

30. (new) The apparatus of claim 29, wherein the gate is substantially perpendicular to the channel.

31. (new) The apparatus of claim 29, wherein a gate oxide is formed between the channel and the gate.